Texas Instruments

DAC5672/62/52

14-Bit, 12-Bit, and 10-Bit Dual Channel DAC EVM

User's Guide

2006

Wireless Infrastructure

SLAU139B

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the specified input and output voltage ranges described in the EVM User's Guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Preface

Read This First

About This Manual

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1 − Introduction
- ❏ Chapter 2 −Circuit Description
- ❏ Chapter 3 − Physical Description and Parts List
- ❏ Chapter 4 − Schematics

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

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Figures

Tables

Chapter 1

Introduction

This user's guide document gives a general overview of the DAC5672/62/52 evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module.

Topic **Page**

1.1 Purpose

The DAC5672/62/52 EVM provides a platform for evaluating the DAC5672/62/52 digital-to-analog converter (DAC) family under various signal, reference, and supply conditions. This document should be used in combination with the EVM schematic diagram supplied.

1.2 EVM Basic Functions

Digital inputs to the DAC can be provided with CMOS level signals up to 275 MSPS through two 34-pin headers. This enables the user to provide high-speed digital data to the DAC5672/62/52.

The analog output from the DAC is available via SMA connectors. Because of its flexible design the analog output of the DAC5672/62/52 can be configured to drive a 50-Ω terminated cable using a 4:1 or 1:1 impedance ratio transformer or single-ended referred to GND.

Power connections to the EVM are via banana jack sockets. Separate sockets are provided for the analog and digital supplies.

In addition to the internal bandgap reference provided by the DAC5672/62/52 device, options are provided on the EVM to allow external reference to be provided to the DAC.

1.3 Power Requirements

The demonstration board requires only two power supplies. The first, +3.3 VA, is required to be +3.3 VDC at banana jack J12 with the return going to J14. This is the analog supply for the DAC5672/62/52. The second, +3.3 VB, is required to be +3.3 VDC at banana jack J13 with the return to J15. This is the digital +3.3-V supply for the DAC5672/62/52. The EVM can be powered using only one supply, but powering from separate supplies will provide higher performance.

Voltage Limits

Exceeding the maximum input voltages can damage EVM components. Undervoltage may cause improper operation of some or all of the EVM components.

The DAC5672/62/52 EVM provides a platform for evaluating the following digital-to-analog devices:

Table 1–1. Device List

DEVICE	RESOLUTION	SAMPLE RATE
DAC5672	14–bit resolution	275 MSPS
DAC5662	12–bit resolution	275 MSPS
DAC5652	10–bit resolution	275 MSPS

1.4 DAC5672/62/52 EVM Operation Procedure

The DAC5672/62/52 EVM can be set up in a variety of configurations to accommodate a specific mode of operation. Before starting evaluation, the user should decide on the configuration and make the appropriate connections or changes. The demonstration board comes with following factory-set configuration:

Single clock source mode using a clock input at J3. Single clock source driving CLK_1, WRT_1, CLK_2, and WRT_2 from WRT_1 input. R14, R16, R19, R24, R26, R28, and J4−J8 not installed.

- Transformer coupled outputs using transformer T1 and T2.
- The converter is set to operate with internal reference.
- Full-scale output current set to 20 ma through R_{BIAS} resistor R1 and R2 (GSET jumper on J11 installed between pins 10 and 11 and W1 and W2 installed).
- The DAC5672/62/52 output is enabled (sleep mode disabled). Sleep jumper on J11 is installed between pins 4 and 5.
- Data input set to dual port mode. Mode jumper on J11 is installed between pins 2 and 3.
- Dual input power supplies required. W9 removed.
- VFUSE function disabled. W3 installed.

Chapter 2

Circuit Description

This chapter gives the circuit description including input clock, input data, output data, reference operations, and sleep mode operation.

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2.1 Schematic Diagram

The schematic diagram for the EVM is attached at the end of this document.

2.2 Circuit Function

The following paragraphs describe the EVM circuits.

2.2.1 Input Clock

The DAC5672/62/52 EVM default operation setting is with a single-ended input clock sent to the DAC5672/62/52. A 3 V_{p-p}, 1.5-V offset, 50% duty cycle external square wave is applied to SMA connector J3. This input represents a 50-Ω load to the source. In order to preserve the specified performance of the DAC5672/62/52 converter, the clock source should feature very low jitter. Using a clock with a 50% duty cycle will give optimum dynamic performance. Options are provided to operate the two DAC's with separate clocks. Another option allows the user to provide separate write enables when using interleave mode. See Table 2−1 for proper board configuration.

2.2.2 Input Data

The DAC5672/62/52 EVM can accept +3.3-V CMOS logic level data inputs through the 34-pin headers J9 and J10 per Table 2−1 and Table 2−2. The user can provide series dampening resistors to minimize digital ringing and switching noise if required. The default values are 0 Ω. An option is also available to provided pulldown resistors to the input data paths. Before using the pulldown resistors, the user must make sure the source providing the input data can drive the load the pulldown resistors adds to the data path.

Table 2−1. Input Connector J1

J9 Pin No.	Description	J9 Pin No.	Description
1	Port 1 Data Bit 13 (MSB)	18	GND
2	GND	19	Port 1 Data Bit 4
3	Port 1 Data Bit 12	20	GND
4	GND	21	Port 1 Data Bit 3
5	Port 1 Data Bit 11	22	GND
6	GND	23	Port 1 Data Bit 2
7	Port 1 Data Bit 10	24	GND
8	GND	25	Port 1 Data Bit 1
9	Port 1 Data Bit 9	26	GND
10	GND	27	Port 1 Data Bit 0
11	Port 1 Data Bit 8	28	GND
12	GND	29	
13	Port 1 Data Bit 7	30	GND
14	GND	31	
15	Port 1 Data Bit 6	32	GND
16	GND	33	
17	Port 1 Data Bit 5	34	GND

Table 2−2. Input Connector J10

J10 Pin No.	Description	J10 Pin No.	Description
1	Port 2 Data Bit 13 (MSB)	18	GND
2	GND	19	Port 2 Data Bit 4
3	Port 2 Data Bit 12	20	GND
4	GND	21	Port 2 Data Bit 3
5	Port 2 Data Bit 11	22	GND
6	GND	23	Port 2 Data Bit 2
7	Port 2 Data Bit 10	24	GND
8	GND	25	Port 2 Data Bit 1
9	Port 2 Data Bit 9	26	GND
10	GND	27	Port 2 Data Bit 0
11	Port 2 Data Bit 8	28	GND
12	GND	29	
13	Port 2 Data Bit 7	30	GND
14	GND	31	
15	Port 2 Data Bit 6	32	GND
16	GND	33	
17	Port 2 Data Bit 5	34	GND

2.2.3 Output Data

The DAC5672/62/52 EVM can be configured to drive a doubly terminated 50-Ω cable or provide unbuffered differential outputs.

2.2.3.1 Transformer Coupled Signal Output

The factory-set configuration of the demonstration board provides the user with a single-ended output signal at SMA connector J5. The DAC5672/62/52 is configured to drive a doubly terminated 50-Ω cable using a 4:1 impedance ratio transformer and the center tap of T1 and T2 connected to ground. When using a 1:1 impedance ratio transformer, configure the EVM per Table 2−3.

Table 2−3. Transformer Output Configuration

Configuration	Components Installed†	Components Not Installed
1:1 Impedance ratio transformer	R3−R8, T1, T2	R9, R11, C7, C8
4:1 Impedance ratio transformer	R3 (100), R4 (100), R5 (100), R6 (100), T1 (4:1), T2 (4:1)	R7, R8, R9, R11, C7, C8

† All component values are per the Schematic, except where shown in parenthesis.

2.2.3.2 Unbuffered Differential Output

To provide unbuffered differential outputs, the EVM must be configured as follows: Remove R7, R8, T1, and T2; Install R10, R12, R15, R18, R25, R29, J5, and J8.

2.2.4 Internal Reference Operation

The full-scale output current is set by applying an external resistor (Rset) between the BIASJ pins of the DAC5672/62/52 and ground. The full-scale output current can be adjusted from 20 mA down to 2 mA by varying Rset or changing the externally applied reference voltage. The full-scale output current, IOUTFS, is defined as follows:

$$IOUT_{FS} = 32 \times \left(\frac{V_{EXTIO}}{R_{set}} \right)$$

where VEXTIO is the voltage at pin EXTIO. This voltage is 1.2 V typical when using the internally provided bandgap reference voltage source. On the DAC5672/62/52 EVM, R1 is used to set the output current of channel A and R2 is used to set channel B.

2.2.5 External Reference Operation

The internal reference can be disabled by simply applying an external reference voltage into the EXTIO pin using Test Point 2. The use of an external reference may be considered for applications that require higher accuracy and drift performance, or to add the ability of dynamic gain control. The reference input has a high impedance and can easily be driven by various sources.

Caution

The specified range for external reference voltages should be observed (see the DAC5672/62/52 data sheet for details).

2.2.6 Sleep Mode

The DAC5672/62/52 EVM provides a means of placing the DAC5672/62/52 into a power-down mode. This mode is activated by placing jumper J11 between pins 5 and 6.

2.2.7 Gain Set

The full-scale output current on the DAC5672/62/52 can be set two ways: both channels independently or simultaneously. For independent gain control, set GSET to a logic low. For simultaneous mode, set GSET to a logic high.

2.2.8 Input Data Mode

The DAC5672/62/52 EVM provides a means of placing the DAC5672/62/52 into a dual port data input mode or interleaved mode. With MODE set to a logic high, the device operates in dual port mode. With MODE set to a logic low, the device operates in interleave mode.

Chapter 3

Physical Description and Parts List

This chapter describes the physcial characteristics and the PCB layout of the EVM and lists the components used on the module.

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3.1 PCB Layout

The EVM is constructed on a 4-layer, 5.1-inch x 4.8-inch, 0.062-inch thick PCB using FR−4 material. Figure 3−1 through Figure 3−4 show the PCB layout for the EVM.

Figure 3−1. Top Layer 1

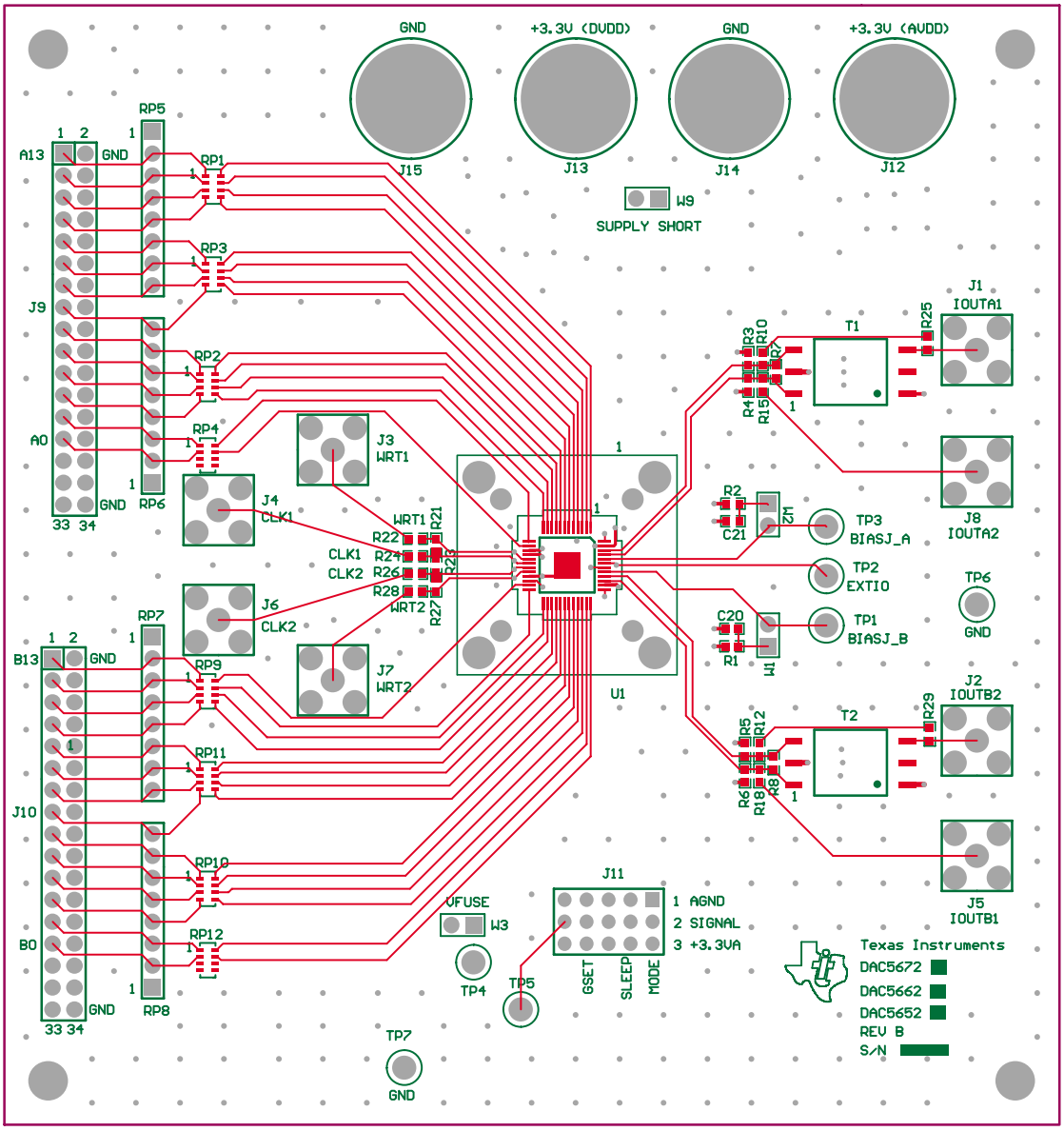


Figure 3−2. Layer 2, Ground Plane

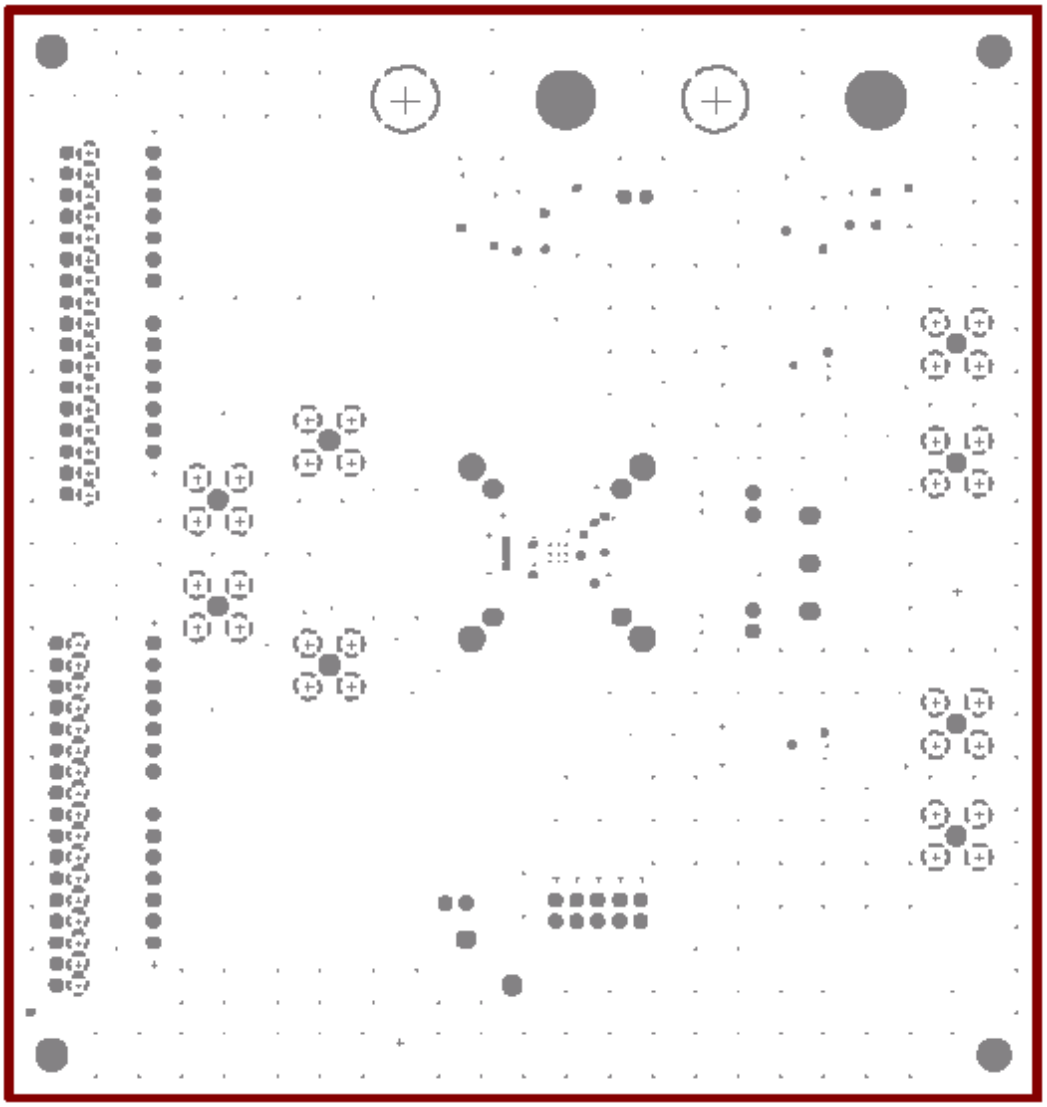


Figure 3−3. Layer 3, Power Plane

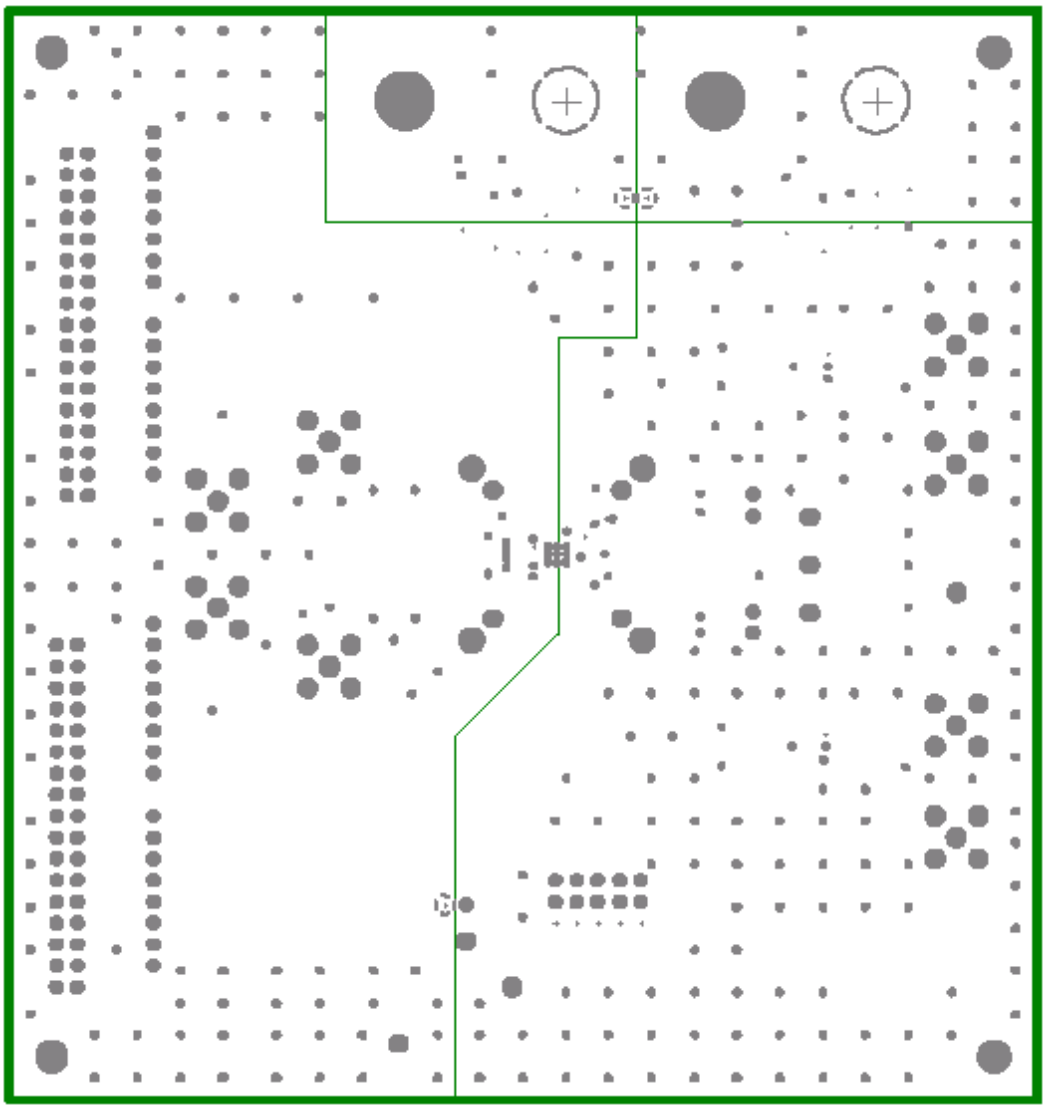
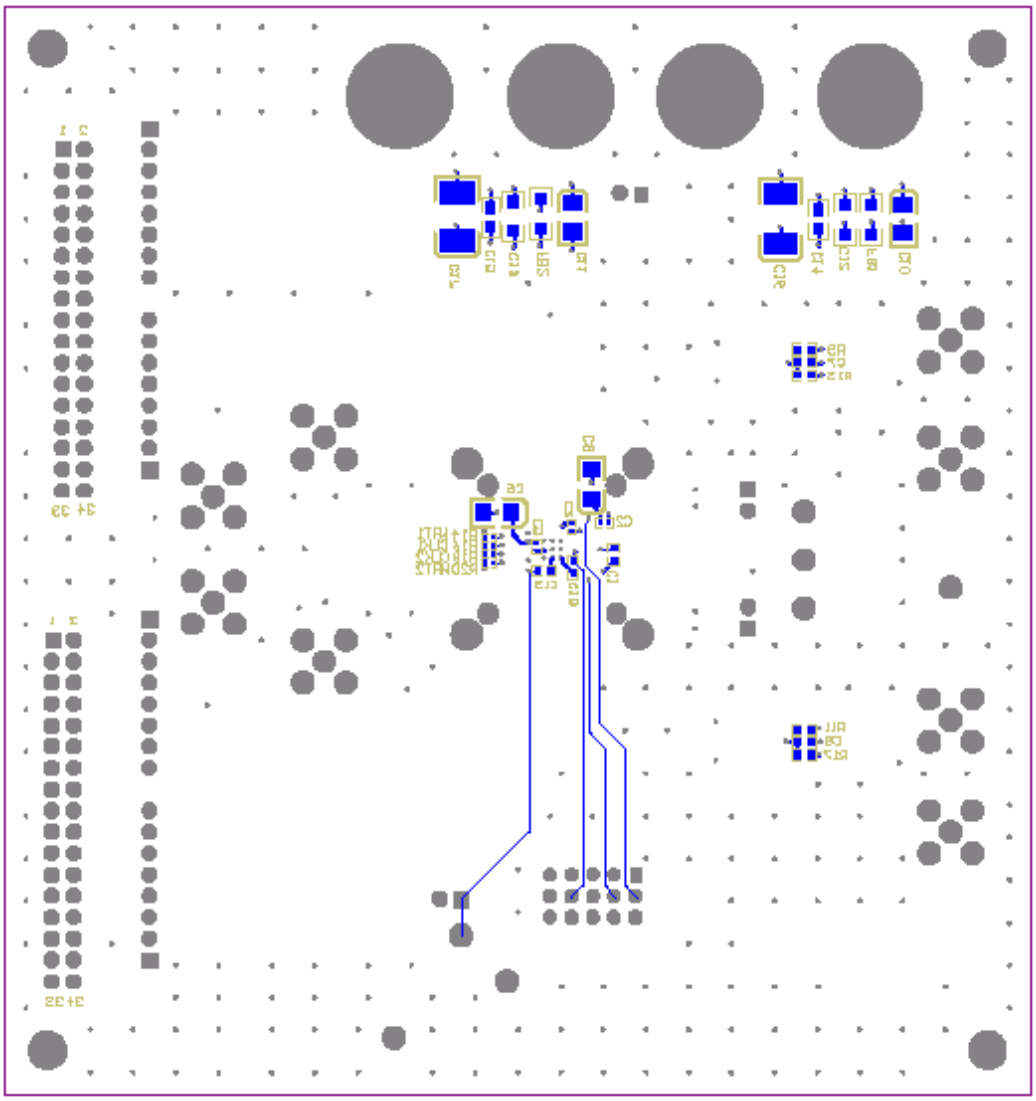


Figure 3−4. Layer 4, Bottom Layer



3.2 Parts List

Table 3–1 lists the parts used in constructing the EVM.

Table 3–1. DAC5672/62/52 EVM Parts List

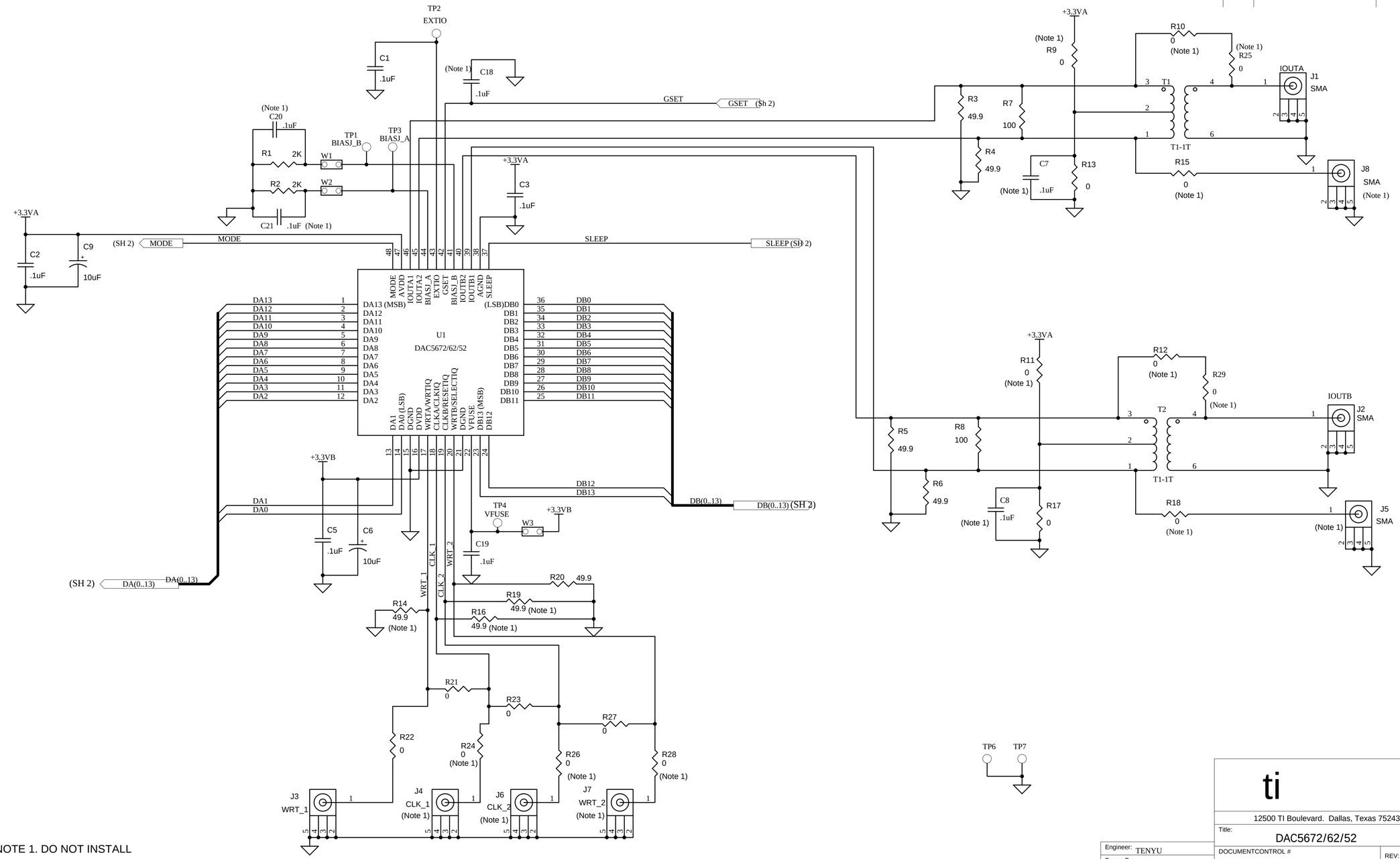
Value	Qty	Part Number	Vendor	Ref Des	Not Installed
Capacitors					
47 μF, tantalum, 10%, 10 V	2	10TPA47M	Sanyo	C16, C17	
10 μF, 10 V, 10% capacitor	4	GRM42X5R106K10	Murata	C6, C9, C10, C11	
1 μF, 16 V, 10% capacitor	2	ECJ–3YB1C105K	Panasonic	C12, C13	
0.01 μF, 50 V,5% capacitor	2	ECJ–2VB1H103K	Panasonic	C14, C15	
0.1 μF, 16 V, 10% capacitor	2	ECJ–1VB1C104K	Panasonic	C1, C19	C7, C8, C18, C20, C21
0.1 μf, 16 V, 80% capacitor	3	ECJ–0EF1C104Z	Panasonic	C2, C3, C5	
Resistors					
0-Ω resistor, 1/16 W, 1%	6	ERJ–3GEY0R00V	Panasonic	R13, R17, R21–R23, R27	R9-R12, R15, R18, R24–R26, R28, R29
100-Ω resistor, 1/16W, 0.1%	2	ERA–3YEB100V	Panasonic	R7, R8	
49.9-Ω resistor, 1/16 W, 1%	4	ERJ–3EKF49R9V	Panasonic	R3, R4, R5, R6	
2-kΩ resistor, 1/16 w, 1%	2	ERJ–3EKF1001V	Panasonic	R1, R2	
49.9-Ω resistor, 1/16 W, 1%	1	ERJ–2RFK49R9X	Panasonic	R20	R14, R16, R19
51–Ω resistor pack	0		CTS		RP5–RP8
0-Ω R–Pack, EXB–38V SERIE	8	EXB–38V000JV	Panasonic	RP1–RP4, RP9-RP12	
Ferrite Beads, Connectors, Jumpers, Jacks, IC's, etc.					
Ferrite bead	2	EXC–ML32A680U	Digi-Key	FB1, FB2	
SMA connectors	3	713–4339 (901–144–8RFX)	Allied	J1, J2, J3	J4, J5, J6, J7, J8
Red test point	5	5000k	Keystone	TP1–TP5	
Black test point	2	5001k	Keystone	TP6, TP7	
2POS_header	4	TSW–150-07–L–S	Samtec	W1 W2 W3 W9	
15-pin header	1	TSW–110-07–L–T	Samtec	J11	
34-pin header	2	TSW–117–07–L–D	Samtec	J9, J10	
Red banana jacks	2	ST–351A	Allied	J12, J13	
Black banana jacks	2	ST–351B	Allied	J14, J15	
DAC5672/62/52	1	DAC5672/62/52IPFB	Texas Instruments	U1	
Transformer	2	T1–1T–KK81	Mini-Circuits	T1, T2	
Install W1, W2; On J11 install jumpers between pins 2 and 3, 4 and 5, and 10 and 11.					

Chapter 4

Schematics

The following pages contain the schematics for the EVM.

Revision History		
REV	ECN Number	Approved



NOTE 1. DO NOT INSTALL

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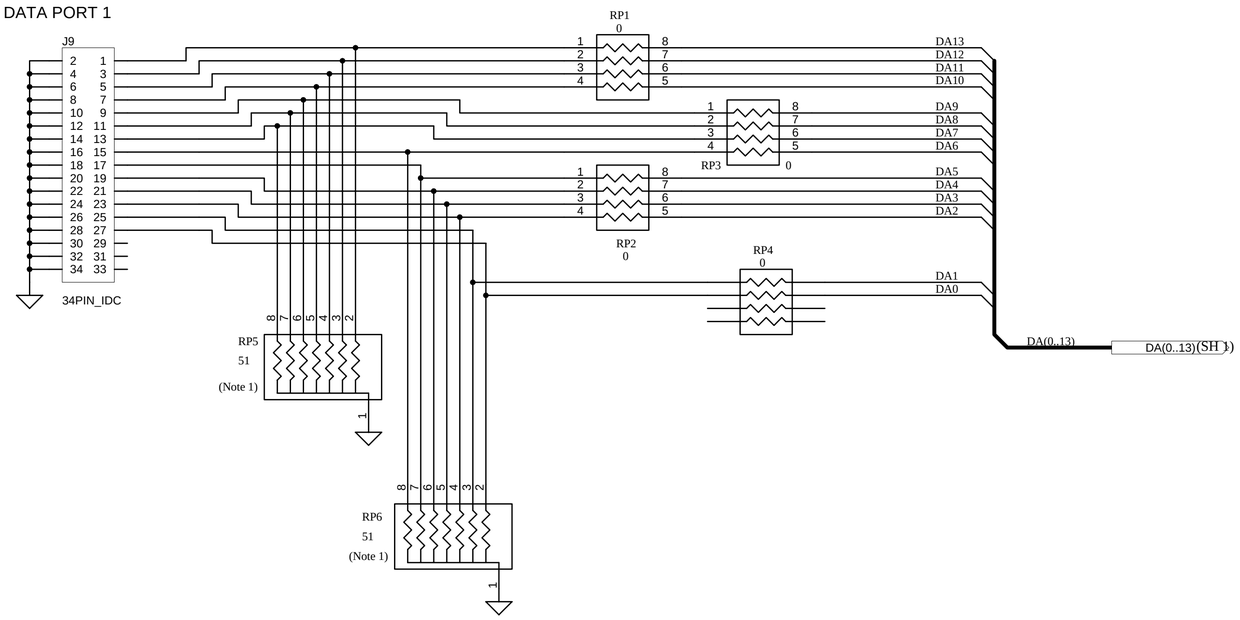
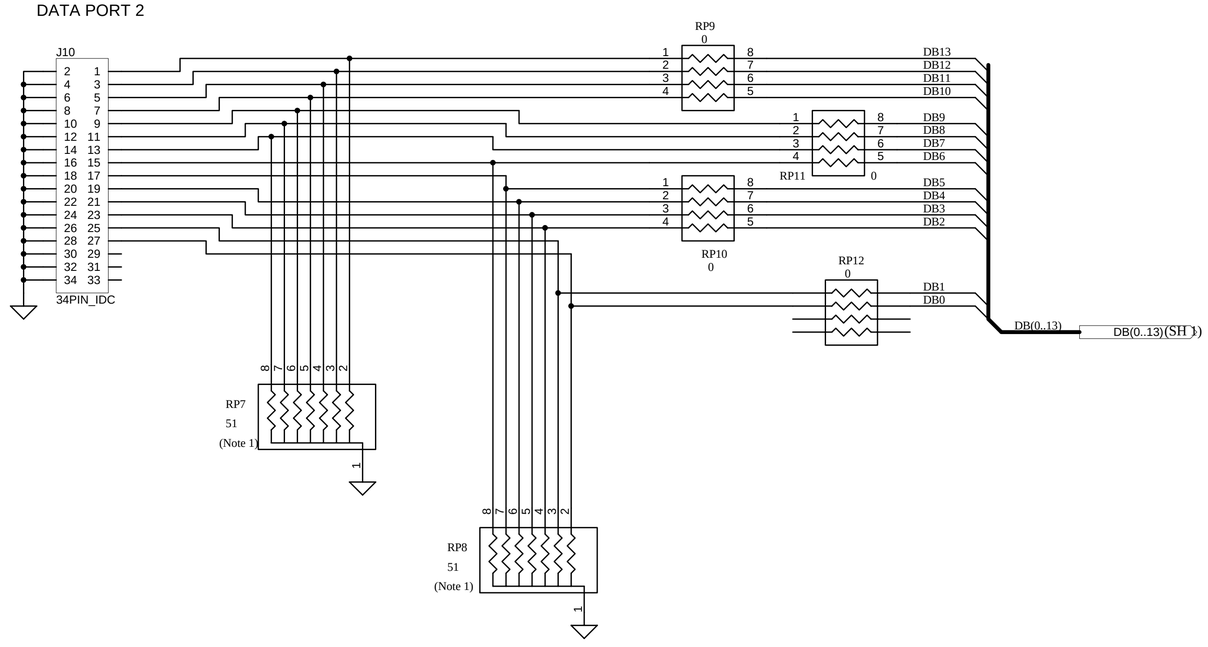
Title: DAC5672/62/52

Engineer: TENYU	DOCUMENTCONTROL #	REV: B	
Drawn By: Y. DEWONCK			
FILE: Sheet1.Sch	DATE: 24-Mar-2006	SIZE: B	SHEET: 1 OF: 2

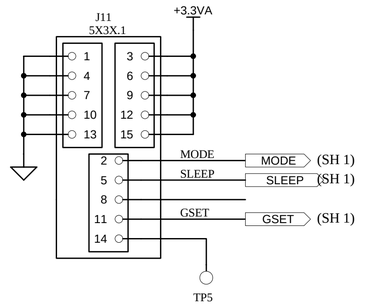
DATA PORT 1



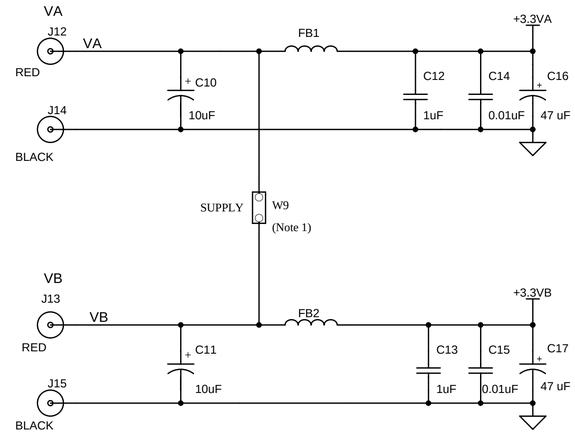
DATA PORT 2



NOTE 1. DO NOT INSTALL



3 ROW 30 PIN CONNECTOR



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